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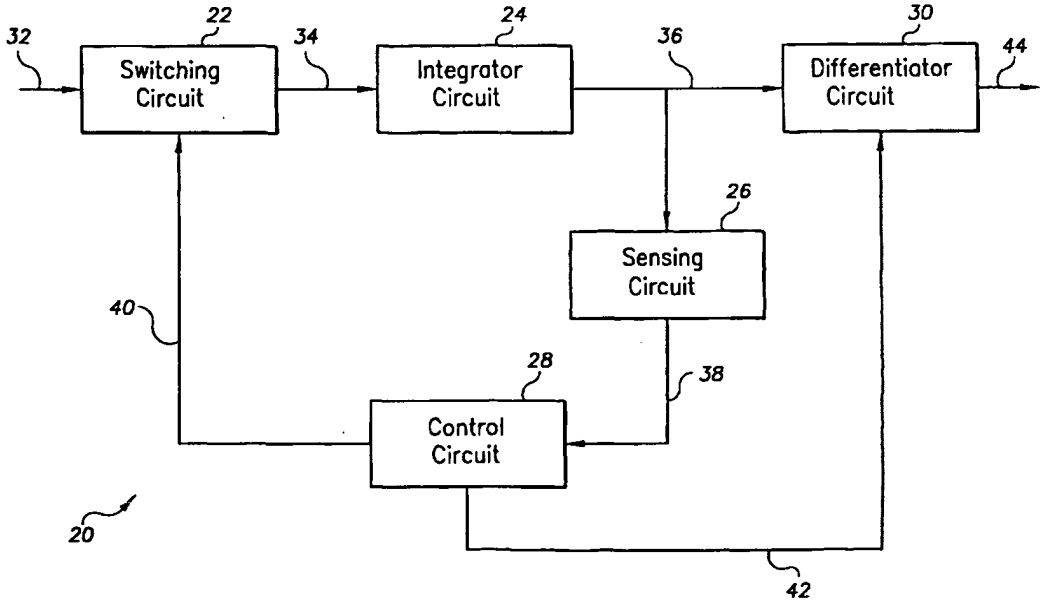
(54) Title: INTEGRATOR TOPOLOGY



(57) Abstract: An apparatus includes a switching circuit, an integrator circuit having an input for receiving a first signal from the switching circuit, a sensing circuit having an input for receiving a second signal from the integrator circuit, and a control circuit having an input for receiving a third signal from the sensing circuit and an output for sending a fourth signal to the switching circuit. In certain applications, the integrator circuit includes a first integrator and a second integrator having an inverting terminal connected to an inverting terminal of the first integrator. The second integrator also includes a non-inverting terminal connected to an output of the first integrator through a first capacitor, and an output connected to a non-inverting terminal of the first integrator through a second capacitor.

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INTEGRATOR TOPOLOGY

BACKGROUND

This invention relates to integrators.

Integrators have high linearity, wide bandwidth, and low noise characteristics. Integrators, however, require a reset interval to discharge the capacitor in the integrator's feedback loop which results in significant "dead" times in measurements and harmful transients on the integrator's input. Additionally, the rapid discharge interval aggravates the problem of dielectric absorption, thereby undermining the lower limit of instrument precision.

Referring to FIG. 1, an integrator 10 includes a feedback loop having a switch 12 in parallel with a feedback capacitor 14. The switch 12 allows the feedback capacitor 14 to discharge when the switch 12 is closed. Placing one or more strings of series resistors and capacitors in parallel with the feedback capacitor 14 with or without the switch 12 reduces at least some of the harmful effects of this discharge. However, even in some arrangements having multiple capacitors, dielectric absorption is still a problem since the charge in the series capacitors is redistributed with the feedback capacitor 14.

SUMMARY

In one general aspect of the invention, an apparatus includes a switching circuit, an integrator circuit having a first input for receiving a first signal from the switching circuit, a sensing circuit having a second input for receiving a second signal from the integrator circuit, and a control circuit having an input for receiving a third signal from the sensing circuit and an output for sending a fourth signal to the switching circuit.

Embodiments of this aspect of the invention may include one or more of the following features. The switching circuit includes two sets of two switches (e.g., MOS devices), the two switches in one set being closed when the two switches in the other set are open.

The integrator circuit includes a first integrator and a second integrator having connected inverting terminals. Each of the first integrator and the second integrator have a non-inverting terminal connected to an output of the switching circuit. Each integrator also has an output connected to the non-inverting terminal of the other integrator through a capacitor.

In operation, the first integrator and the second integrator have voltages on respective ones of the inverting and non-inverting terminals which are substantially equal and have output voltages which are complementary.

The apparatus can be used in a wide variety of applications in which low level, precise measurements are required. For example, in one biological application, the first integrator and the second integrator are operated to each introduce an output voltage into a chemical bath on either side of a biological membrane. In this application, the integrator circuit is configured to detect fluctuations of ion channels. In another application, the integrator circuit may be configured for charge detection.

The sensing circuit includes two comparators, each comparator having an inverting terminal connected to the output of an integrator in the integrator circuit and each comparator having a non-inverting terminal for receiving a threshold voltage.

The control circuit includes a D-type flip-flop and a NAND gate having an output connected to a clock terminal of the D-type flip-flop. The NAND gate includes a pair of

inputs, each connected to an output of a comparator in the sensing circuit.

In this embodiment, the sensing circuit includes an output connected to the D-type flip-flop to change the state of the D-type flip-flop. The D-type flip-flop includes high and low outputs which correspond to two switching positions of switches in the switching circuit.

The apparatus further includes a differentiator circuit having a fourth input for receiving a fifth signal from the integrator circuit and a fifth input for receiving a sixth signal from the control circuit.

The differentiator circuit includes an inverting terminal and a non-inverting terminal, each connected to an output of one of two integrators in the integrator circuit. In operation, the differentiator circuit receives the complementary voltages output by the integrator circuit and provides a demodulated differentiation bit stream representing the slope of the complementary voltages.

Where a differentiator circuit is used, the control circuit provides the sixth signal which determines which output of which integrator in the integrator circuit that each inverting and non-inverting terminal is connected to.

Among other advantages, the apparatus serves as a chopper stabilizer circuit that minimizes the need for rapid discharging of feedback capacitors in the integrator circuit. This feature is provided by alternating the signal current from the switching circuit to the integrator circuit. Thus, the integrator circuit is allowed to perpetually integrate these incoming current signals (low-level transducer signals) and output a continuous flow of two complementary voltages. In one mode of operation, the sensing circuit detects when one of the complementary voltages reaches a threshold value and notifies the control circuit. The control circuit then

responds by sending a signal to the switching circuit. This signal changes the position of switches in the switching circuit, thereby alternating the signal current to the integrator circuit.

In summary, the apparatus eliminates dead time and input transients, compensates for charge injection at the input, and reduces the harmful effects of dielectric absorption. At the same time, the apparatus maintains high linearity, low noise, and wide bandwidth.

In another aspect of the invention, an integrator circuit includes a first integrator and a second integrator having an inverting terminal connected to an inverting terminal of the first integrator. The second integrator also includes a non-inverting terminal connected to an output of the first integrator through a first capacitor, and an output connected to a non-inverting terminal of the first integrator through a second capacitor.

In still another aspect of the invention, a differentiator circuit includes a first input for receiving one of a first signal or a second signal; a second input for receiving the other of the first signal or the second signal; and a third input for receiving a third signal. The third signal determines which of the first input or second input receives the first signal and which of the first input or second input receives the second signal.

Embodiments of this aspect of the invention may include one or more of the following additional features. The first and second signals are complementary voltage signals. The first input and the second input are each connected to an output of an integrator. The third signal includes an output of a control circuit.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the

description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic diagram of a conventional integrator.

FIG. 2 is a block diagram of a chopper stabilizing circuit.

FIG. 3 is a schematic diagram of the block diagram of FIG. 2.

FIG. 4 is a graph showing the output of the integrator circuit of FIG. 3.

FIGS. 5-6 are graphs showing the chopper stabilization of the integrator circuit of FIG. 3.

FIG. 7 is an unfolded view of the integrator circuit of FIG. 3.

FIGS. 8-9 are graphs showing the output of the integrator circuit of FIG. 3.

FIGS. 10-11 are graphs showing the response of the integrator of FIG. 3 to input current.

FIGS. 12-13 are graphs showing the charge injection compensation of the integrator circuit of FIG. 3.

FIG. 14 is a graph showing currents detectable by the integrator circuit of FIG. 3.

FIG. 15 is a graph showing charge detection by a conventional integrator circuit.

FIG. 16 is a graph showing charge detection by the integrator circuit of FIG. 3.

FIG. 17 is a schematic diagram of the differentiator circuit of FIG. 2.

DETAILED DESCRIPTION

Referring to FIG. 2, a chopper stabilizing circuit 20 includes a switching circuit 22, an integrator circuit 24, a sensing circuit 26, a control circuit 28, and a differentiator circuit 30. In general, the chopper stabilizing circuit 20 has a topology and is controlled in a manner that eliminates the need for rapid discharging of feedback capacitors in the integrator circuit 24. In particular, and as will be discussed in greater detail below, this advantage is accomplished by alternating the signal current from the switching circuit 22 to the integrator circuit 24. In this way, the integrator circuit 24 can perpetually integrate these incoming current signals (low-level transducer signals) and output a continuous flow of two complementary voltages. The sensing circuit 26 detects when one of the complementary voltages reaches a threshold value and notifies the control circuit 28. The control circuit 28 responds by sending a signal to the switching circuit 22. This signal changes the position of switches in the switching circuit 22, thereby alternating the signal current to the integrator circuit 24. The differentiator circuit 30 receives the complementary voltages output by the integrator circuit 24 and provides a demodulated differentiation bit stream representing the slope of the complementary voltages. As will be described in more detail below, this chopper stabilizing circuit 20 eliminates dead time and input transients, compensates for charge injection at the input, and reduces the harmful effects of dielectric absorption. At the same time, the chopper stabilizing circuit 20 maintains high linearity, low noise, and wide bandwidth.

In the layout of the chopper stabilizing circuit 20, the switching circuit 22 has an input at a first node 32 for receiving an input signal. The input signal includes the

driving current/voltage for the chopper stabilizing circuit 20 from a load, a current source, and/or a voltage source. The switching circuit 22 has an output at a second node 34 that is determined by the position of the switch(es) included in the switching circuit 22. The integrator circuit 24 has an input at the second node 34 for receiving an input signal from the switching circuit 22 and an output at a third node 36. The sensing circuit 26 has an input at the third node 36 for receiving an input signal from the integrator circuit 24 and an output at a fourth node 38. The control circuit 28 has an input at the fourth node 38 for receiving an input signal from the sensing circuit 26 and output at a fifth node 40 and a sixth node 42. The switching circuit 22 has an input for receiving an input signal from the control circuit 28 at the fifth node 40. This input signal controls the position of the switch(es) in the switching circuit 22.

The differentiator 30 is shown in FIG. 2, though its presence is not necessary to ensure proper functioning of the chopper stabilizing circuit 20. If it is not present, the integrator circuit 24 and the control circuit 28 may not necessarily have outputs at the third node 36 and the sixth node 42, respectively. The differentiator circuit 30 has an input at the third node 36 for receiving an input signal from the integrator circuit 24 and at the sixth node 42 for receiving an input signal from the control circuit 28. The input signal at the sixth node 42 controls the switch(es) included in the differentiator circuit 30. The differentiator also has an output at a seventh node 44.

Referring to FIG. 3, one particular embodiment of a chopper stabilizing circuit 20 includes a switching circuit 22, an integrator circuit 24, a sensing circuit 26, and a control circuit 28. The chopper stabilizing circuit 20 eliminates the need for rapid discharging of feedback

capacitors 60a-b (preferably Teflon®) in the integrator circuit 24 by alternating the signal current from the switching circuit 22 to two integrators 62a-b included in the integrator circuit 24. In this way, one feedback capacitor discharges while the other charges, thereby providing two inversely related output voltages (Vout+, Vout-) at Vout nodes 36a-b. Once either of the output voltages reaches a predetermined threshold value (Vth), a regenerative comparator 76a-b included in the sensing circuit 26 and connected to this output voltage is tripped. Hysteresis prevents the sensing circuit 26 from causing false resets. The comparator 76a-b triggers a D-type flip-flop 78 through a NAND gate 79, both included in the control circuit 28. As the flip-flop 78 changes state, the outputs Q and Q-bar connected to the switches 66a-b, 68a-b cause them to reverse position. This reversal preserves the same orientation with respect to the load 72, maintaining a uniform bias, while alternating the signal current to the integrator circuit 24.

More specifically, the switching circuit 22 includes two pairs of two symmetric switches 66a-b, 68a-b. The switches 66a-b, 68a-b may be any type of standard MOS (metal oxide semiconductor) switch, e.g., MAXIM 326. Only one set of switches 66a-b, 68a-b is closed at a time, each closed switch providing a path for a signal to the non-inverting input terminal of an operational amplifier (opamp) 70a-b, e.g., Burr-Brown OP627, included in the integrators 62a-b. When the phase one (>1) switches 66a-b are closed, a load 72 provides the input current (Io) to the first opamp 70a while a voltage source 74 provides the bias voltage (Vb) to the second opamp 70b. When the phase two (>2) switches are closed, the load 72 and the voltage source 74 provide current/voltage to the other opamp 70a-b. The values of

Vout+ at the Vout node 36a and Vout- at the Vout node 36b depend on the position of these switches 66a-b, 68a-b.

FIG. 4 shows the inverse relationship between Vout+ (Vcf2) and Vout- (Vcf1). In this scenario, the >2 switches 68a-b begin closed and the feedback capacitors 60a-b initially are discharged, so Vout+ and Vout- begin at Vb. When Io flows through the load 72, Vout+ and Vout- alternately and inversely ramp up and down in accordance with:

$$\frac{dV}{dt} = \frac{Io}{Cf}$$

When Io decreases at a time t1, this relationship ceases.

The integrator circuit 24 can effectively integrate forever (constantly flowing Io), with negligible glitching during phase switching. This lack of glitch is helped by the symmetry of input stage of the integrator circuit 24. Every input stage node 80a-c sees one switch 66a-b, 68a-b turn on and another turn off during a phase transition. The already low charge injection of the switches 66a-b, 68a-b is then effectively reduced to tens of femtoCoulombs (fC). Additionally, the symmetric pair requires no voltage drop across a switch 66a-b, 68a-b, aiding in keeping leakage currents below a picoAmp (pA). The voltages at the input stage nodes 80a-c are substantially the same.

Referring to FIGS. 5 and 6, it is appreciated that offset may be a problem as in FIG. 5, but techniques exist to alleviate this problem, e.g., a stabilizing circuit. FIG. 5 shows the chop before stabilization, and FIG. 6 shows the chopper stabilization of the integrator circuit 24.

Referring to FIG. 7, an unfolded view of the integrator circuit 24 helps demonstrate the manner in which the circuit

functions. The compensation of the integrator circuit 24 may be broken down into two sections: minor and major loops. The minor loop concerns the stability of each opamp 70a-b; the major loop comprises the total feedback loop around the integrator. The major loop encompasses a unity gain inverter with a voltage divider formed by the first feedback capacitor 60a reacting with the capacitance off the input stage of the first opamp 70a. The input capacitance is dominated by the opamp input capacitance and the parasitics of the switches 66a-b, 68a-b. The ratio of the capacitive voltage divider in this embodiment is approximately ten, which will keep the major loop crossover well below that of the minor loops. The minor loops are stabilized with the addition of shunt capacitances 82a-b, which help compensate for phase lag due to shunt resistors 84a-b (preferably metal film) reacting with the input capacitance of the opamps 70a-b. With the bandwidth of the opamps 70a-b on the order of 10MHz in this embodiment, the chopper stabilizing circuit 20 should be able to track currents with a bandwidth of approximately 1MHz.

FIGS. 8-13 further demonstrate the functioning of the integrator circuit 24. FIG. 8 shows Vout+ and Vout- with 50μs per horizontal division, the typical reset duration in standard integrators, e.g., Axopatch 200B and nuclear physics instrumentation. FIG. 9 shows a zoom in on the reset transient, with the switching occurring of the order of 500ns, e.g., 700ns. The 2pF feedback capacitor 60a-b and a residual voltage jump of 20mV signifies under 40fC of charge injection. FIG. 10 shows the response of the integrator circuit 24 (top trace) to input current (bottom trace), a 2nA peak-to-peak triangle wave. Because of this response, the integrator circuit 24 could be used for direct digitization of input current via single-slope integration by measuring the period between resets. FIG. 11 shows the response of the

integrator circuit 24 in FIG. 10 superimposed with a 100kHz sinusoid supplied by a 2pF capacitor at the input. FIG. 12 shows the charge injection before compensation, and FIG. 13 shows the charge injection after compensation by the integrator circuit 24.

Now referring to FIG. 14, the integrator circuit 24 can be used to detect the fluctuations of ion channels important in cell signaling and biological transport. These currents range from 0.1pA to 100pA, with bandwidths of 10kHz. The integrator circuit 24 allows for measuring these currents without glitches from resetting.

Now referring to FIGS. 15 and 16, the integrator circuit 24 can also be used for charge detection. For example, x-ray and particle detectors output charge pulses that are usually integrated. Whenever a conventional integrator hits a limit value as in FIG. 15, it must reset and data can be lost. Using the integrator circuit 24, the dead-time (lost data) is greatly reduced by the absence of capacitor resets as shown in FIG. 16.

A differentiator circuit 30, shown in FIG. 17, may be part of a chopper stabilizing circuit. The differentiator circuit 30 includes two switches 92a-b. The switches 92a-b may be any type of standard MOS (metal oxide semiconductor) switch, e.g., MAXIM 326. Each switch 92a-b is either in a horizontal (>1) position, e.g., switch 92a from a top start node 94a to a top end node 96a, or a diagonal (>2) position, e.g., switch 92a from the top start node 94a to a bottom end node 96b, at any given time. Each closed switch 92a-b provides a path for a signal at entering nodes 36a-b to travel to the inverting terminal or to the non-inverting terminal of an opamp 100. Input from a control circuit (not shown) determines the position of the switches 92a-b. If the

differentiator circuit is connected to the chopper stabilizing circuit 20 (see FIG. 2), the output from the control circuit 78 provides the phase information for the switches 92a-b.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. An apparatus, comprising:
a switching circuit;
an integrator circuit having a first input for receiving a first signal from the switching circuit;
a sensing circuit having a second input for receiving a second signal from the integrator circuit; and
a control circuit having a third input for receiving a third signal from the sensing circuit and an output for sending a fourth signal to the switching circuit.

2. The apparatus of claim 1 wherein the switching circuit includes two sets of two switches, the two switches in one set being closed when the two switches in the other set are open.

3. The apparatus of claim 2 wherein the switches are MOS devices.

4. The apparatus of claim 1 wherein the integrator circuit includes a first integrator and a second integrator, the first integrator and the second integrator having connected inverting terminals, each of the first integrator and the second integrator having a non-inverting terminal connected to an output of the switching circuit, and each having an output, each output connected to the non-inverting terminal of the other integrator through a capacitor.

5. The apparatus of claim 4 wherein, in operation, the first integrator and the second integrator have voltages on respective ones of the inverting and non-inverting terminals which are substantially equal.

6. The apparatus of claim 4 wherein, in operation, the first integrator and the second integrator have output voltages which are complementary.

7. The apparatus of claim 4 wherein, in operation, the first integrator and the second integrator are each configured to introduce an output voltage into a chemical bath on either side of a biological membrane.

8. The apparatus of claim 4 wherein the integrator circuit is configured to detect fluctuations of ion channels.

9. The apparatus of claim 4 wherein the integrator circuit is configured for charge detection.

10. The apparatus of claim 1 wherein the sensing circuit includes two comparators, each comparator having an inverting terminal connected to the output of an integrator in the integrator circuit and each comparator having a non-inverting terminal connected to a threshold voltage.

11. The apparatus of claim 1 wherein the control circuit includes a D-type flip-flop and a NAND gate having an output connected to a clock terminal of the D-type flip-flop.

12. The apparatus of claim 11 wherein the NAND gate includes a pair of inputs, each connected to an output of a comparator in the sensing circuit.

13. The apparatus of claim 11 wherein the sensing circuit includes an output connected to the D-type flip-flop to change the state of the D-type flip-flop.

14. The apparatus of claim 11 wherein the D-type flip-flop includes high and low outputs which correspond to two switching positions of switches in the switching circuit.

15. The apparatus of claim 1 further comprising a differentiator circuit having a fourth input for receiving a fifth signal from the integrator circuit and a fifth input for receiving a sixth signal from the control circuit.

16. The apparatus of claim 15 wherein the differentiator circuit includes an inverting terminal and a non-inverting terminal, each connected to an output of one of two integrators in the integrator circuit.

17. The apparatus of claim 16 wherein the control circuit provides the sixth signal which determines which output of which integrator in the integrator circuit that each inverting and non-inverting terminal connects to.

18. An integrator circuit, comprising:

a first integrator; and

a second integrator having an inverting terminal connected to an inverting terminal of the first integrator, a non-inverting terminal connected to an output of the first integrator through a first capacitor, and having an output connected to a non-inverting terminal of the first integrator through a second capacitor.

19. The integrator circuit of claim 18 wherein the first integrator and the second integrator each have their respective non-inverting terminal connect to a different switch in a switching circuit.

20. The integrator circuit of claim 18 wherein, in operation, the first integrator and the second integrator have voltages on their respective ones of the inverting and non-inverting terminals which are substantially equal.

21. The integrator circuit of claim 18 wherein, in operation, the first integrator and the second integrator have output voltages which are complementary.

22. The integrator circuit of claim 18 wherein, in operation, the first integrator and the second integrator each have an output voltage which goes into a chemical bath on either side of a biological membrane.

23. The integrator circuit of claim 18 wherein the integrator circuit is configured to detect fluctuations of ion channels.

24. The integrator circuit of claim 18 wherein the integrator circuit is configured for charge detection.

25. A differentiator circuit, comprising:

a first input for receiving one of a first signal or a second signal;

a second input for receiving the other of the first signal or the second signal; and

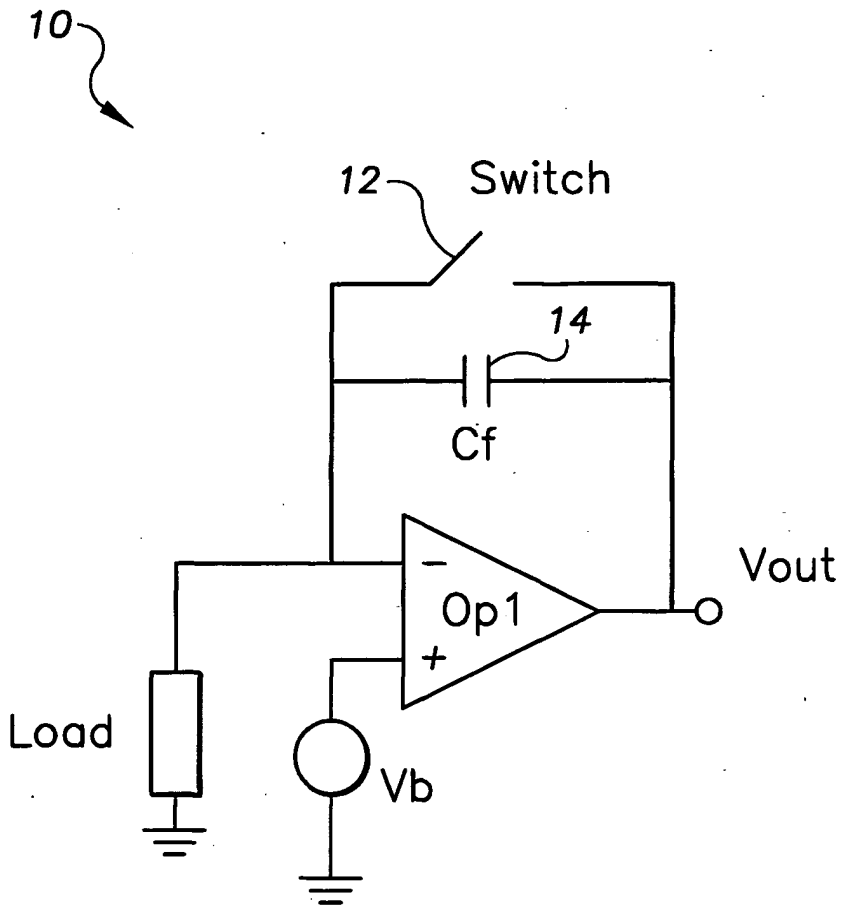
a third input for receiving a third signal, the third signal determining which of the first input or second input receives the first signal and which of the first input or second input receives the second signal.

26. The differentiator circuit of claim 26 wherein the first and second signals are complementary voltage signals.

27. The differentiator circuit of claim 26 wherein the first input and the second input are each connected to an output of an integrator.

28. The differentiator circuit of claim 26 wherein the third signal includes an output of a control circuit.

FIG. 1
PRIOR ART



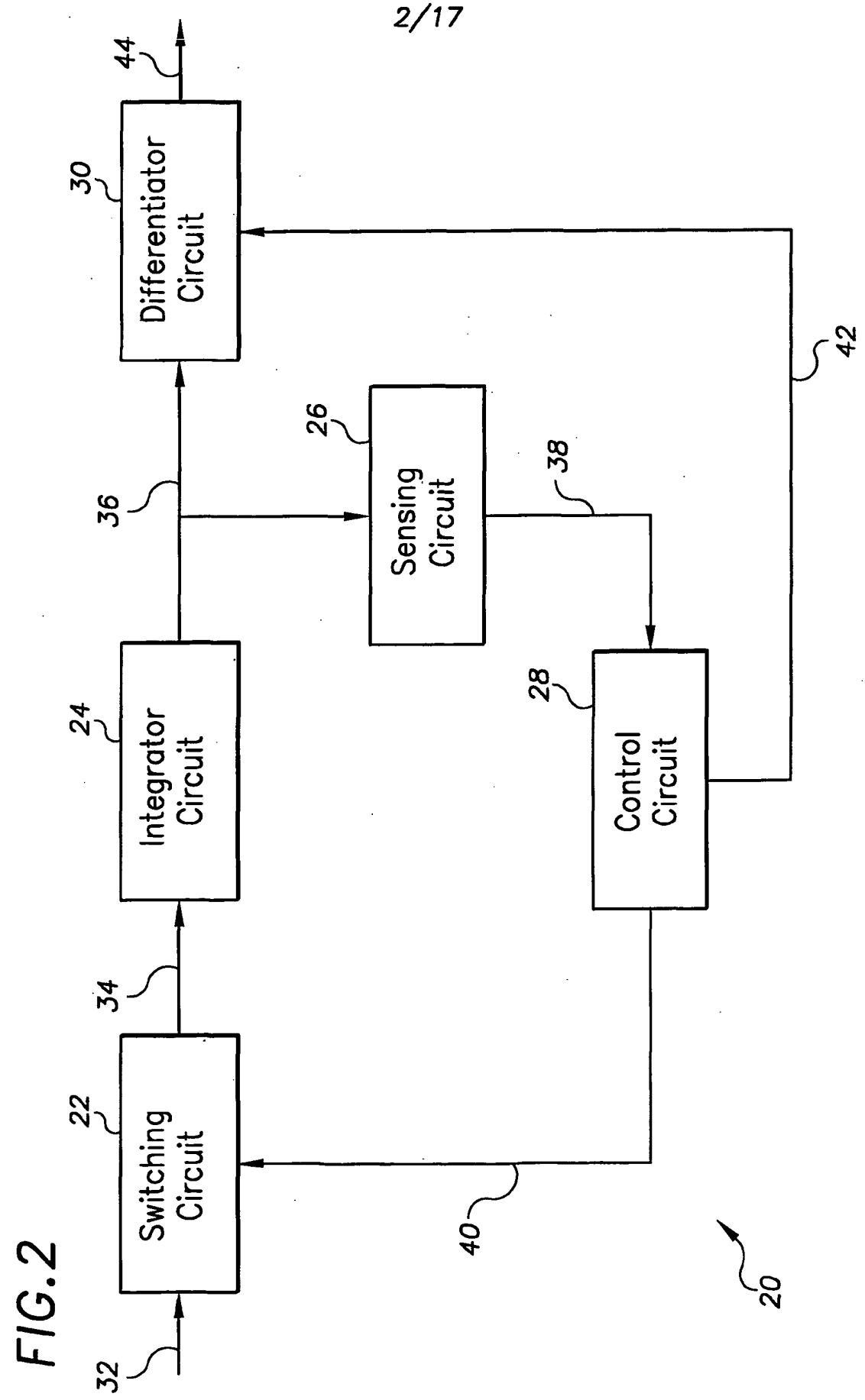
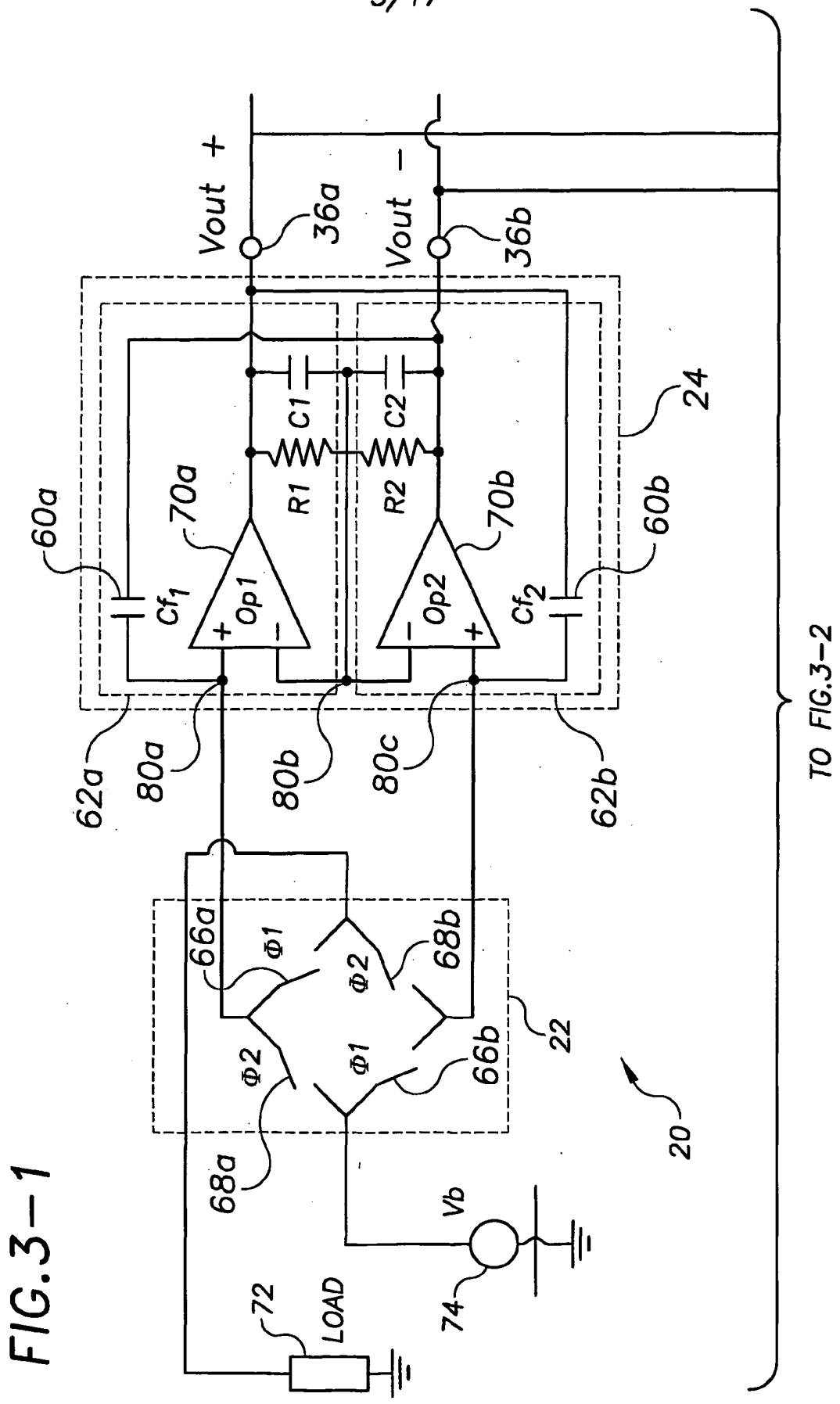

Differentiator Circuit
30
44
42
Sensing Circuit
26
38
36
Integrator Circuit
24
Control Circuit
28
Switching Circuit
22
34
40
20
32

FIG.2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Vout −
36a
36b
C1
C2
R1
R2
24
60a
60b
70a
70b
Cf1
Cf2
Op1
Op2
62a
62b
80a
80b
80c
66a
66b
68a
68b
Φ1
Φ2
22
20
Vb
74
72
LOAD
TO FIG.3-2

FIG.3-1

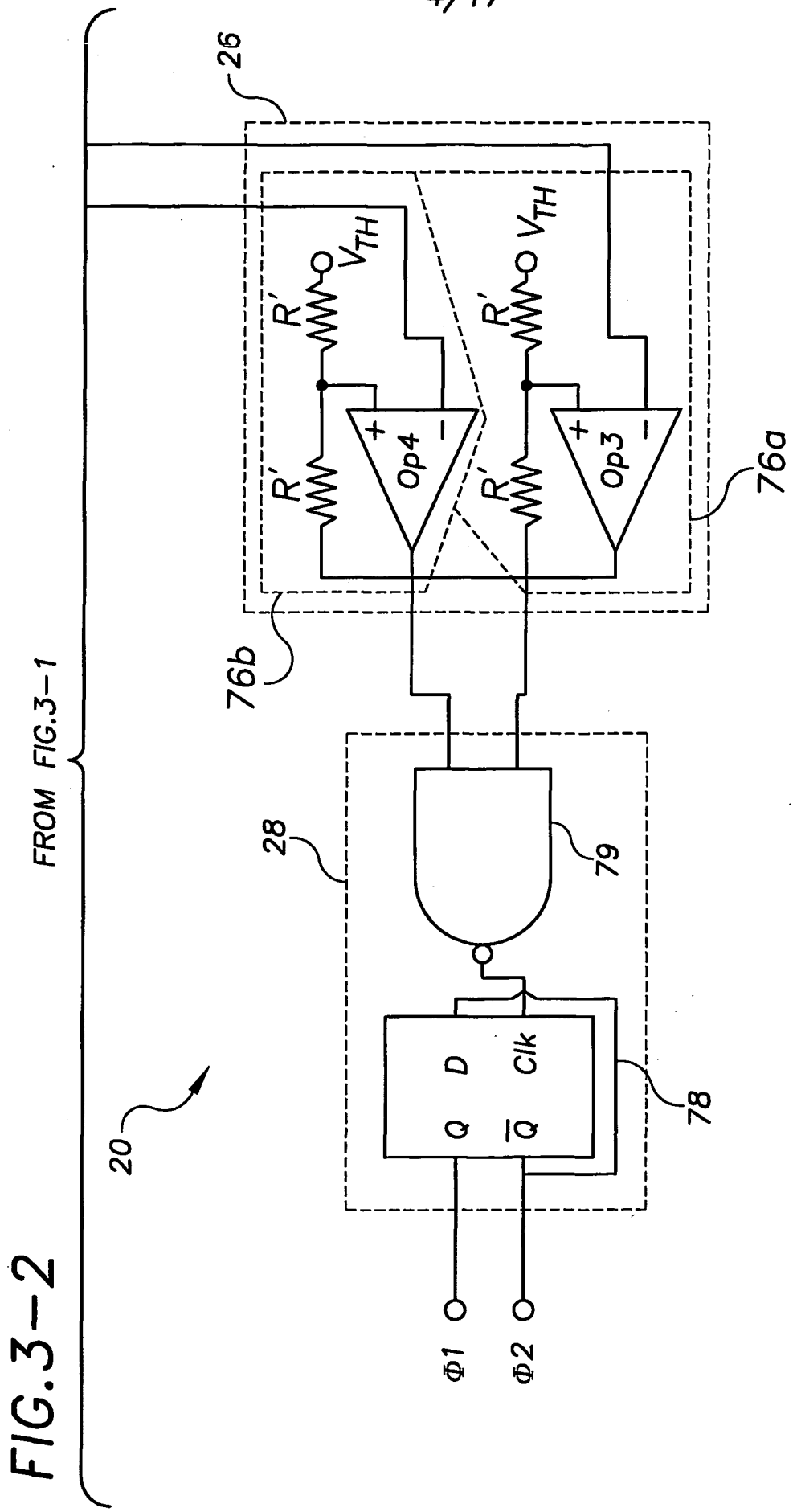


FIG.3-2

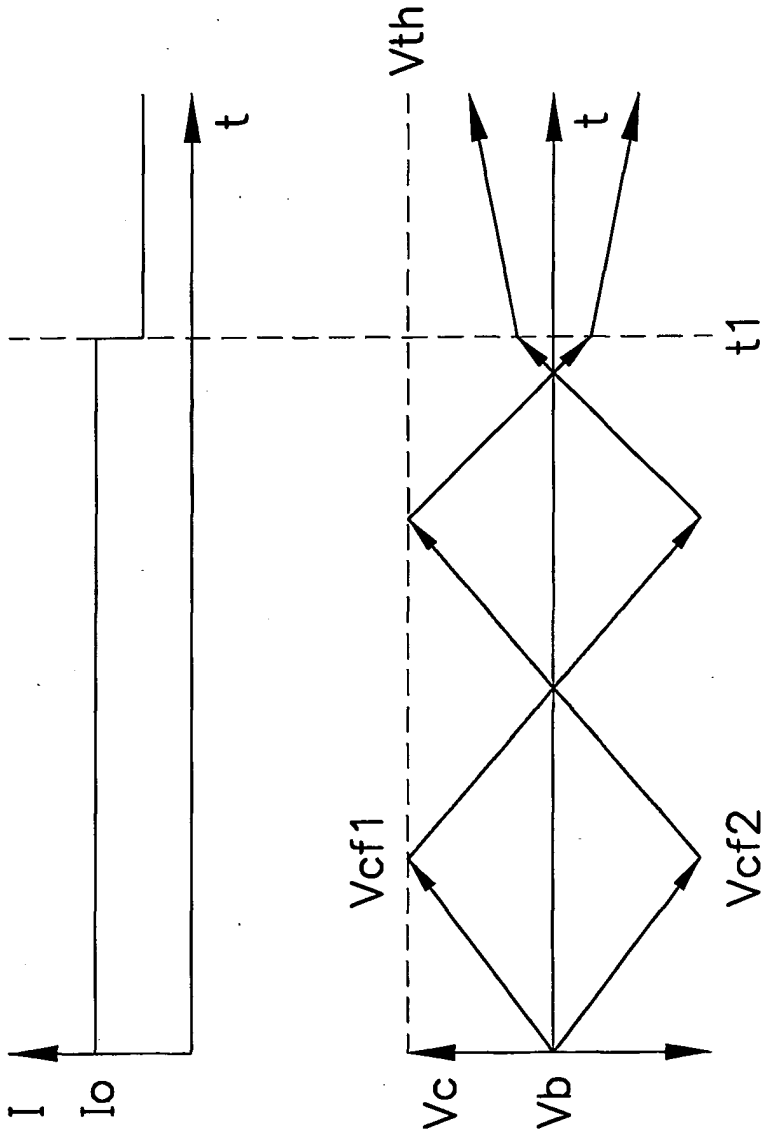


FIG. 4

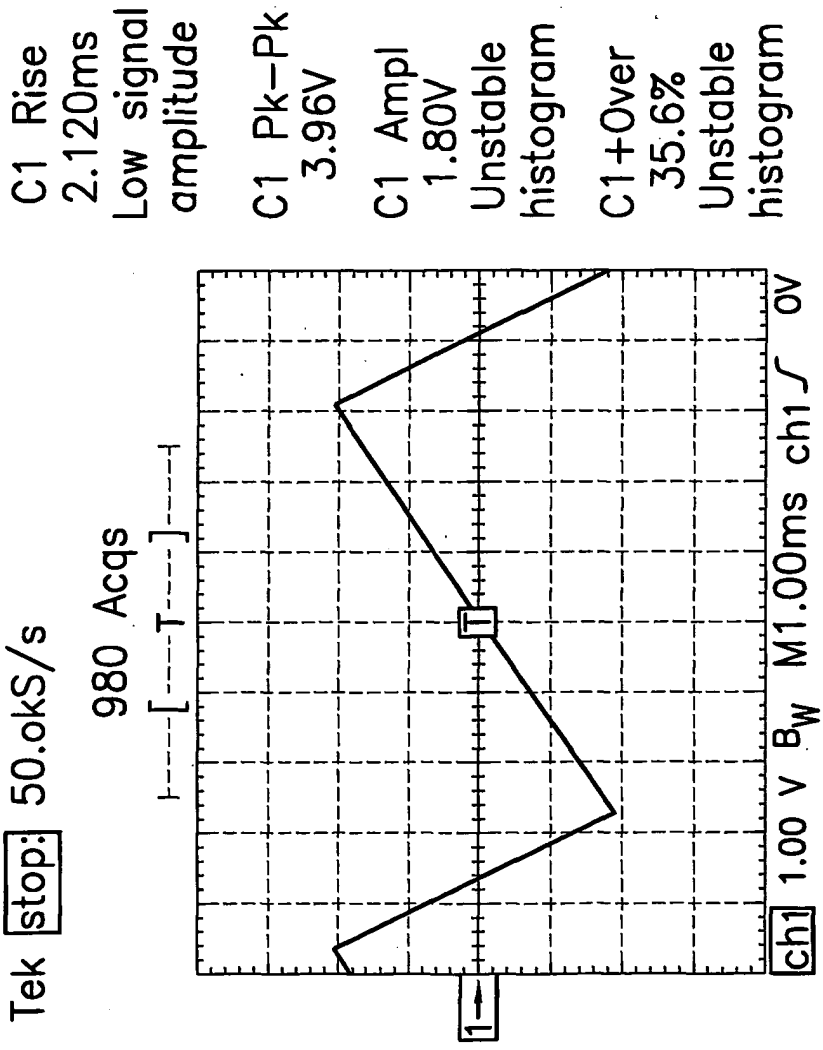
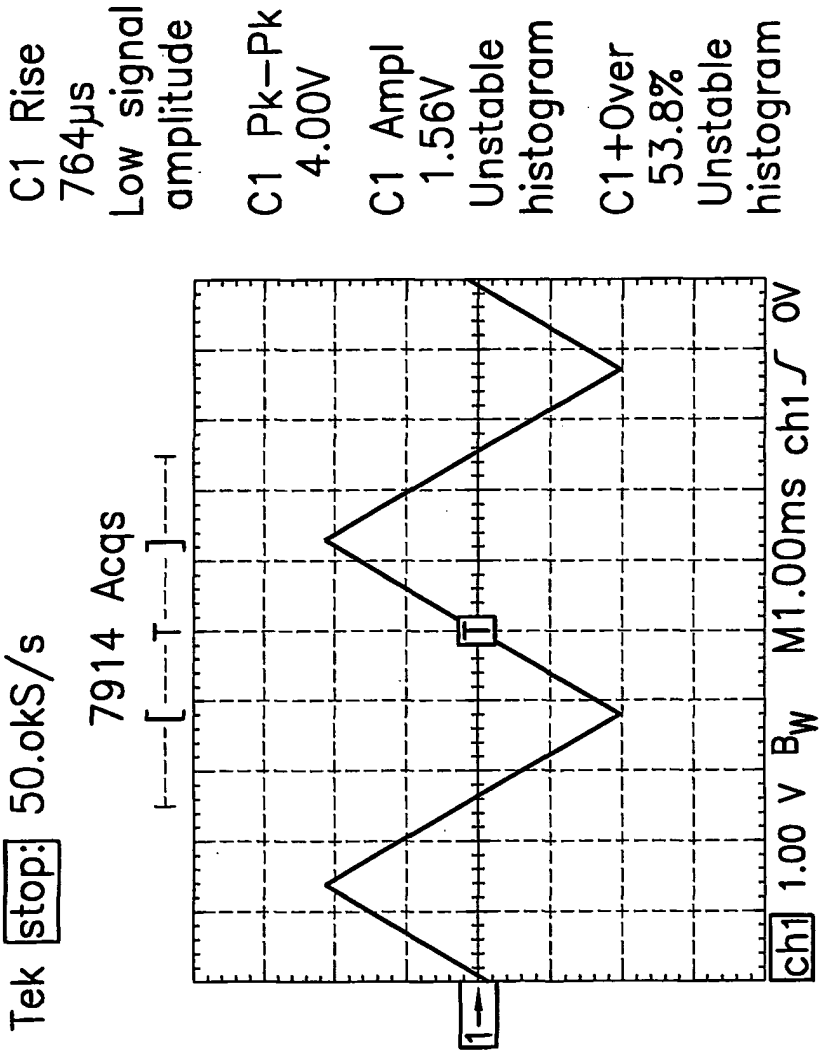

C1 Rise
2.120ms
Low signal
amplitude
C1 Pk-Pk
3.96V
C1 Ampl
1.80V
Unstable
histogram
C1+Over
35.6%
Unstable
histogram
Tek stop: 50.0kS/s
980 Acqs
ch1 1.00 V BW M1.00ms ch1 0V

FIG.5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C1 Ampl
1.56V
Unstable
histogram
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Unstable
histogram
Tek stop: 50.0kS/s
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ch1 1.00 V BW M1.00ms ch1 0V

FIG.6

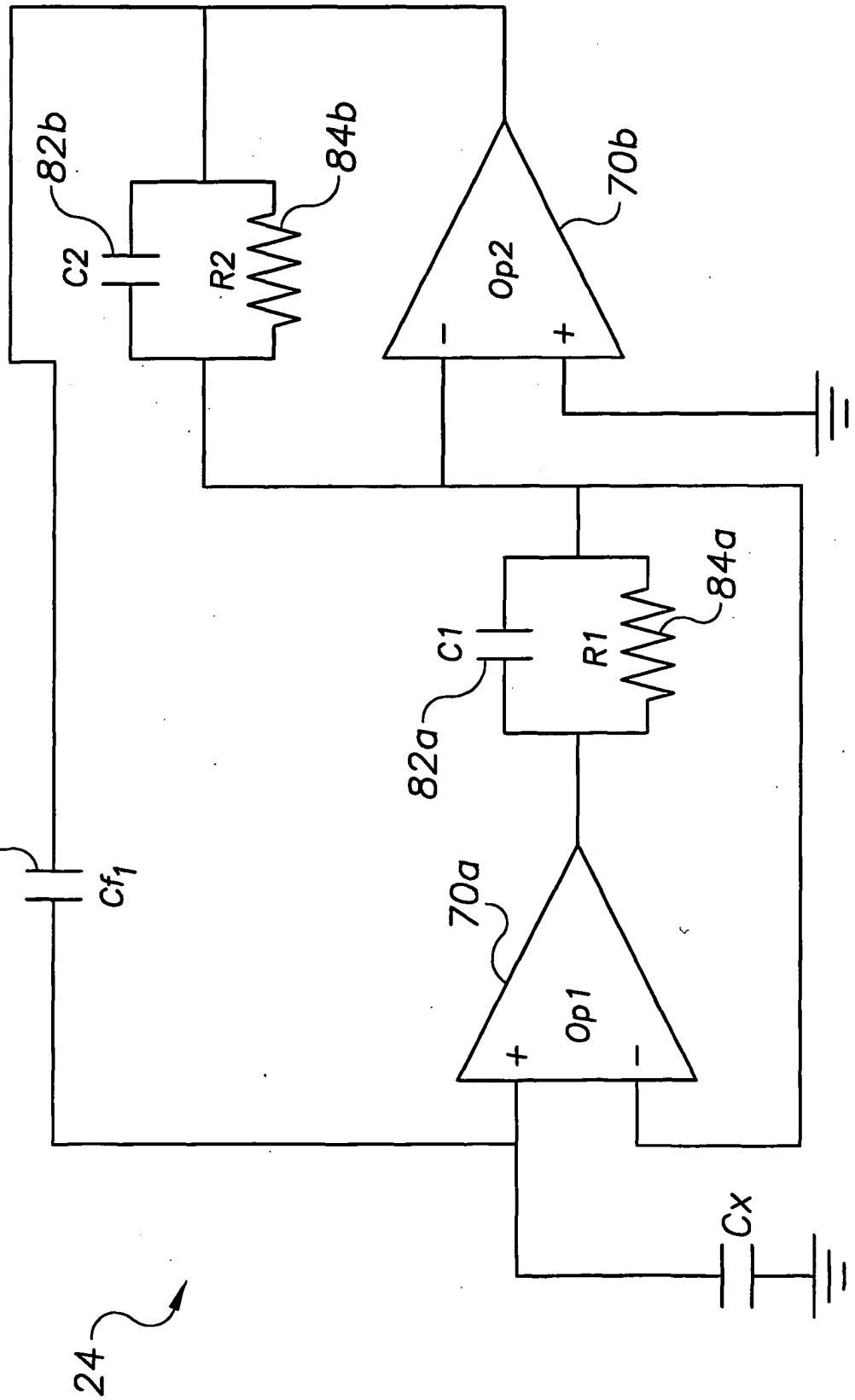


FIG. 7

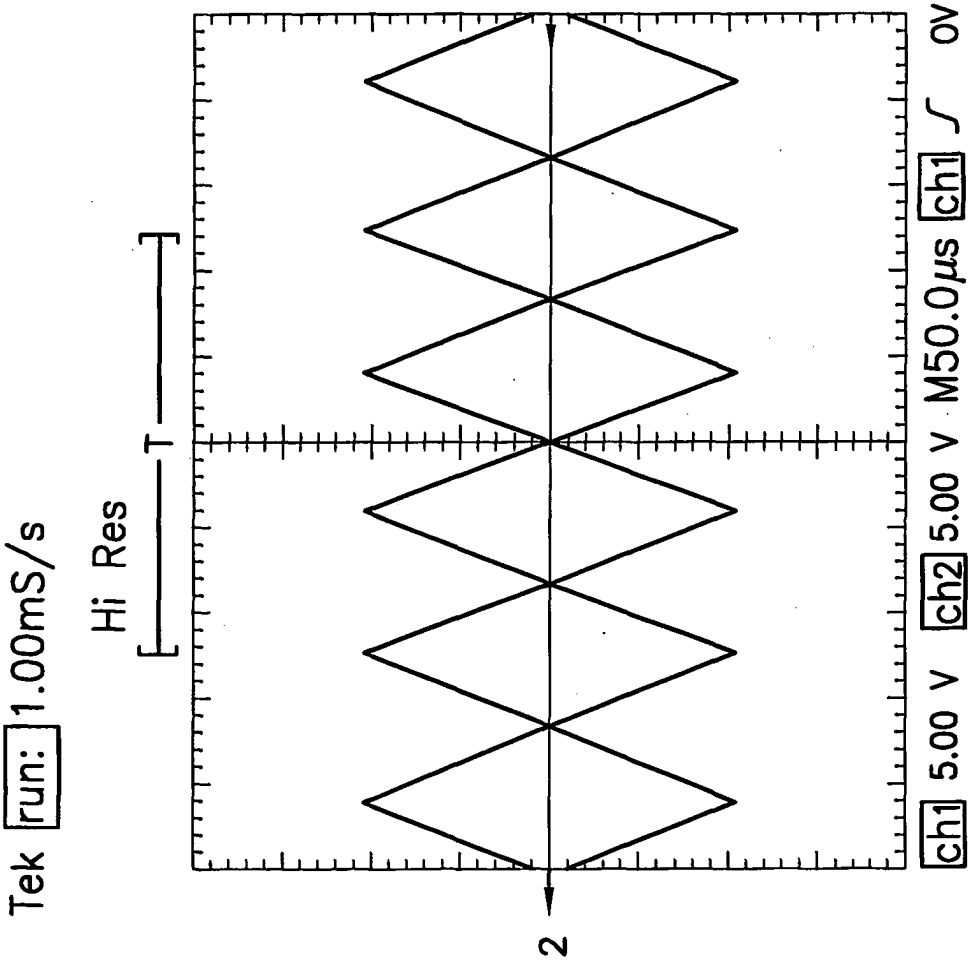


FIG.8

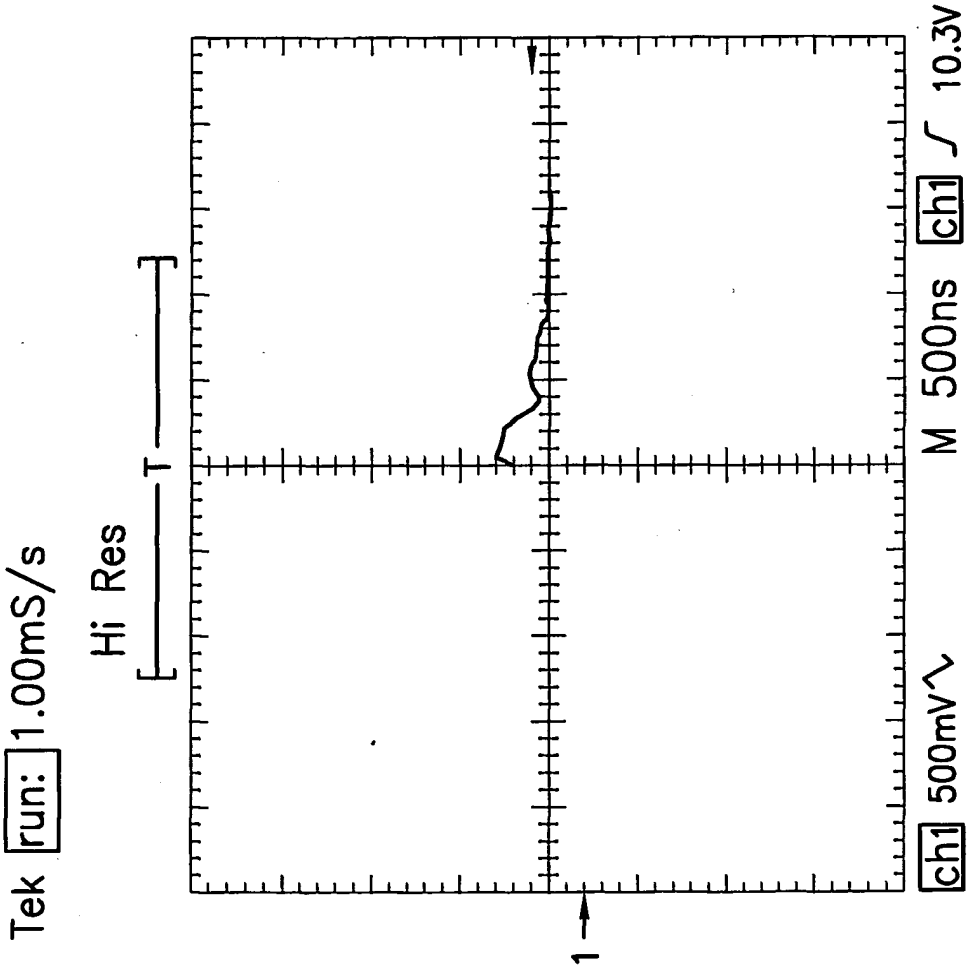


FIG. 9

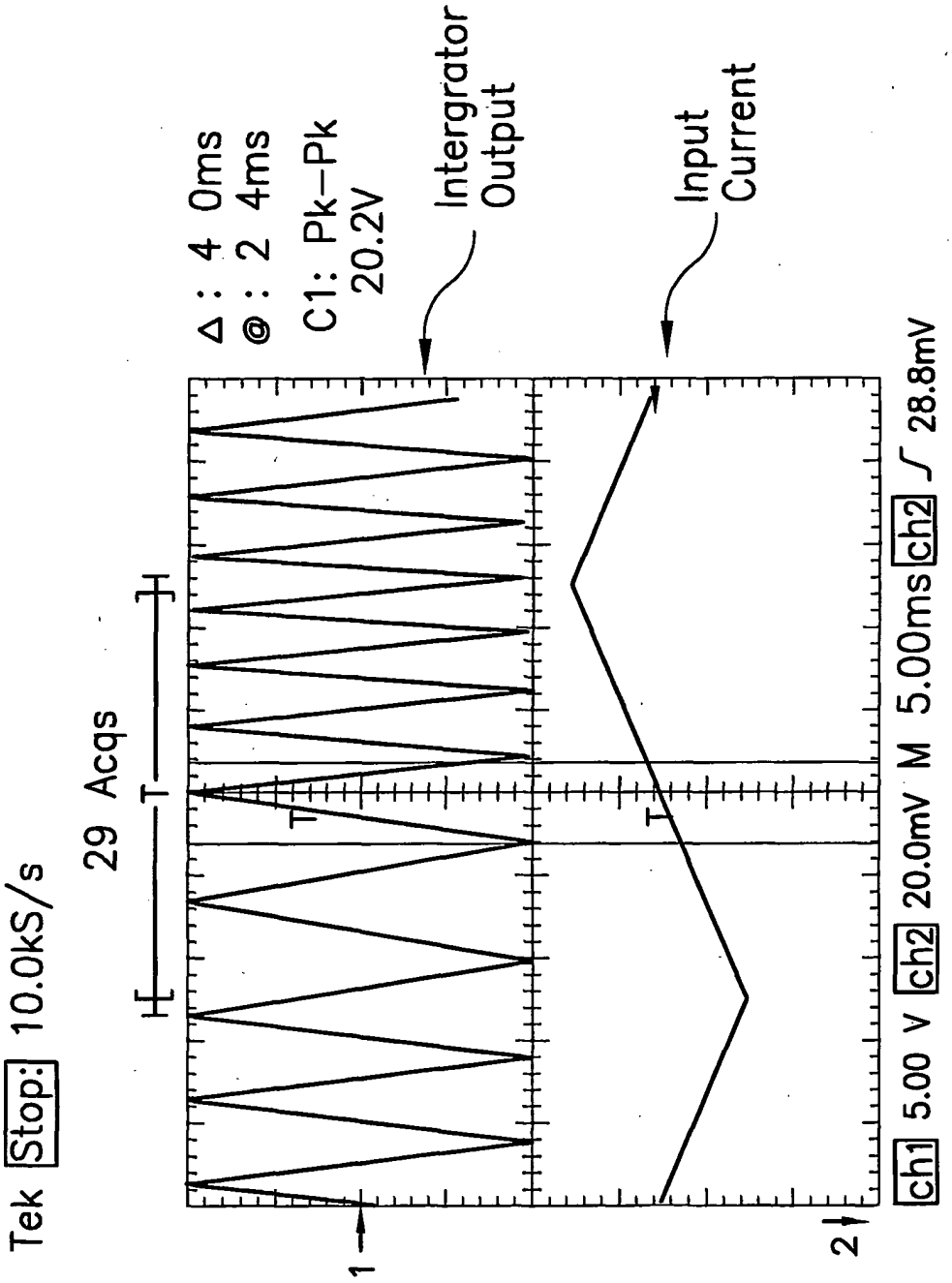

Tek Stop: 10.0kS/s
29 Acqs
Δ : 4 0ms
@ : 2 4ms
C1: Pk–Pk
20.2V
Intergrator
Output
Input
Current
ch1 5.00 V ch2 20.0mV M 5.00ms ch2 ∫ 28.8mV
1
2

FIG. 10

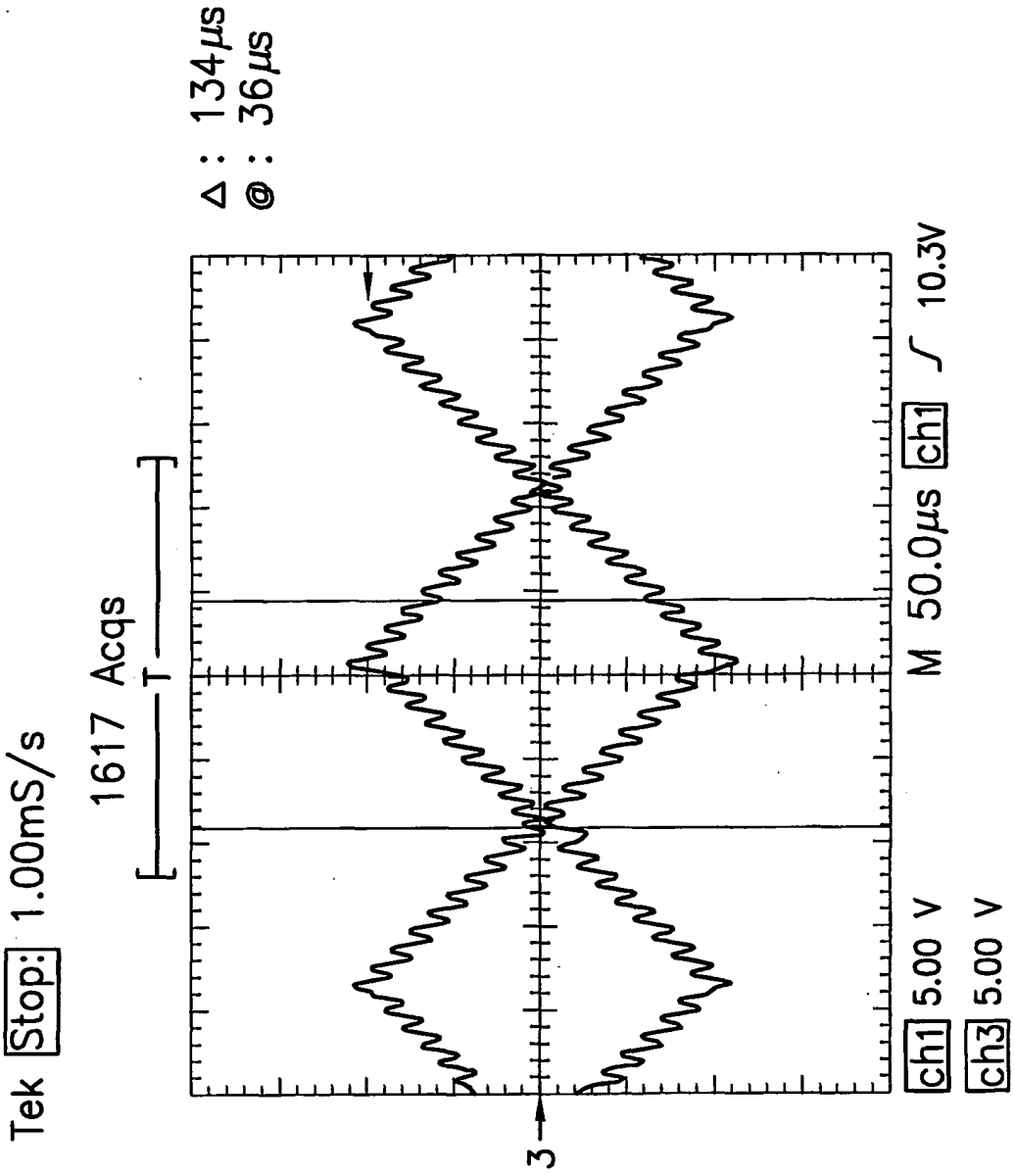

Tek Stop: 1.00mS/s
1617 Acqs
Δ : 134µs
@ : 36µs
M 50.0µs ch1 ∫ 10.3V
ch1 5.00 V
ch3 5.00 V
3

FIG. 11

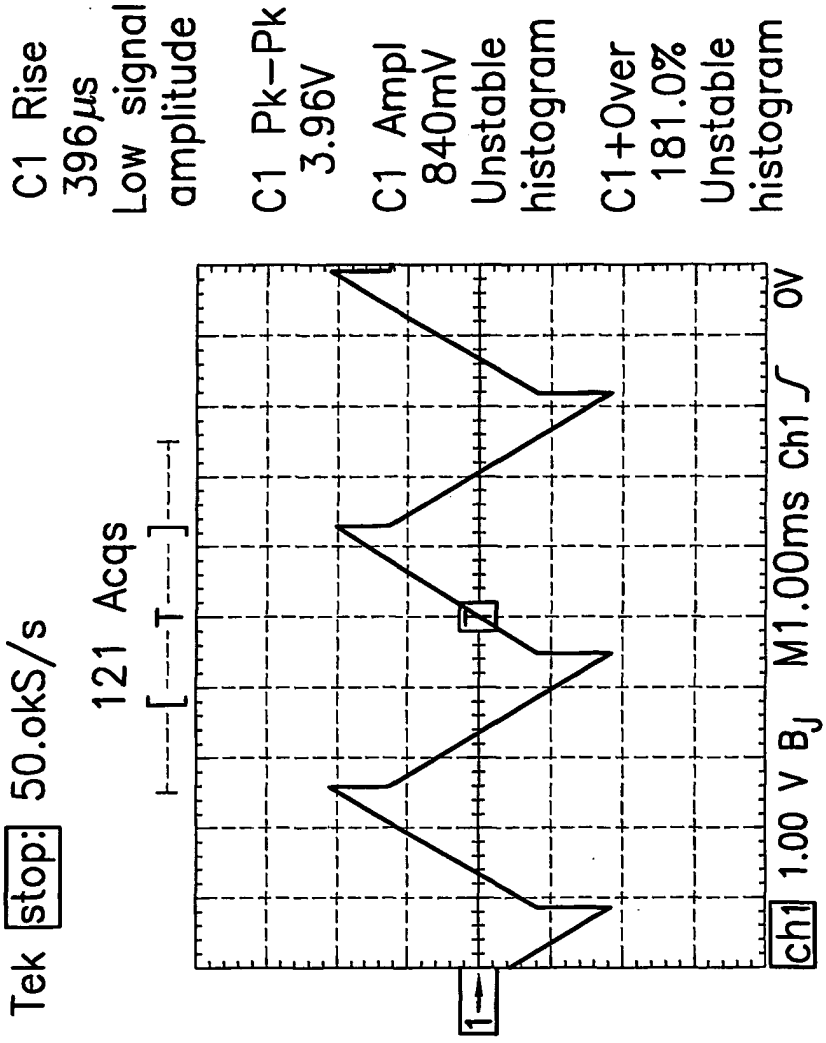

Tek stop: 50.0kS/s
121 Acqs
C1 Rise
396µs
Low signal
amplitude
C1 Pk-Pk
3.96V
C1 Ampl
840mV
Unstable
histogram
C1+Over
181.0%
Unstable
histogram
ch1 1.00 V BJ M1.00ms Ch1 ∫ 0V

FIG. 12

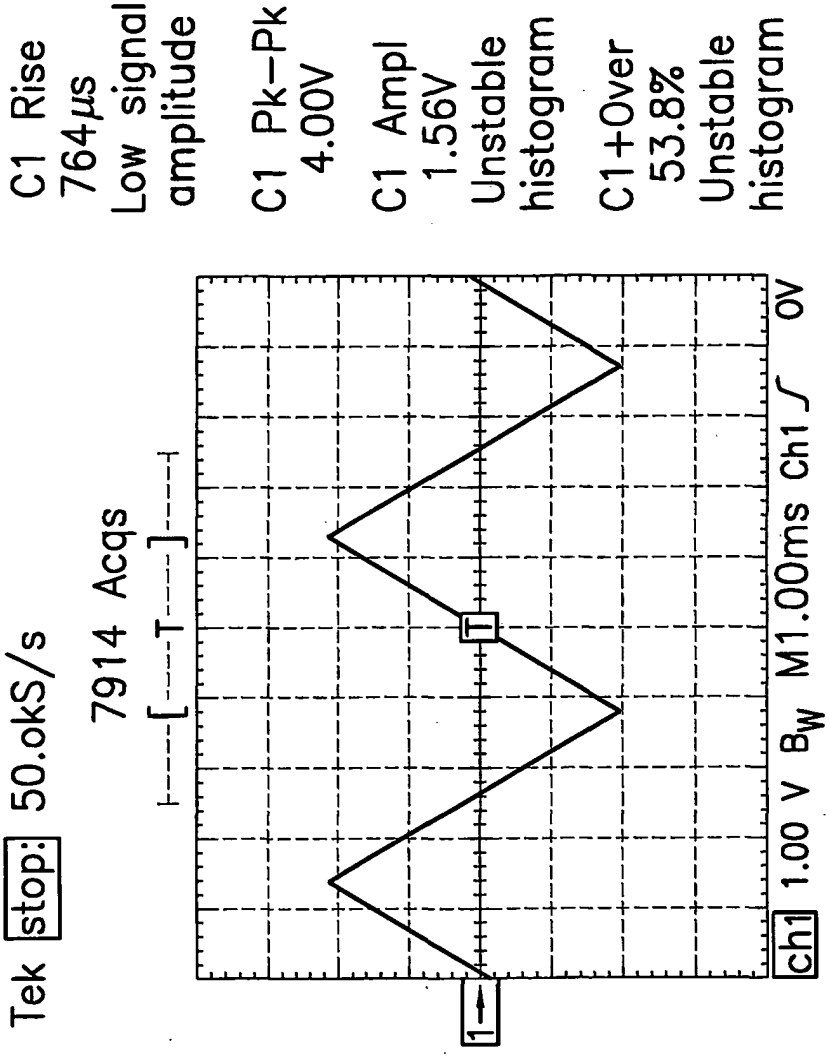

C1 Rise
764µs
Low signal
amplitude
C1 Pk–Pk
4.00V
C1 Ampl
1.56V
Unstable
histogram
C1+Over
53.8%
Unstable
histogram
Tek stop: 50.0kS/s
7914 Acqs
ch1 1.00 V BW M1.00ms Ch1 0V

FIG. 13

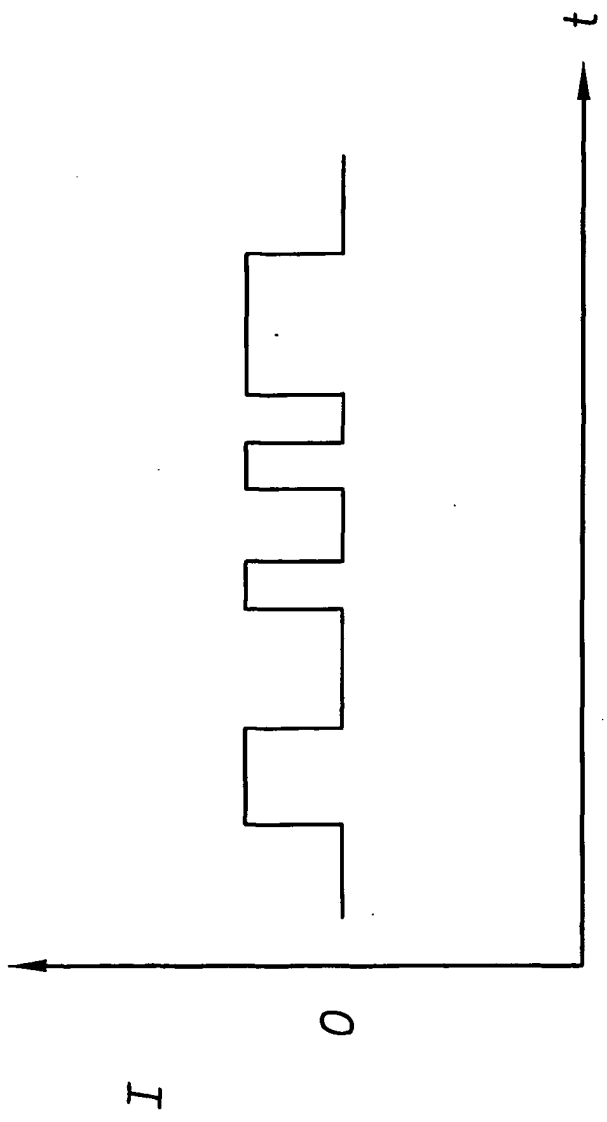


FIG. 14

FIG. 15

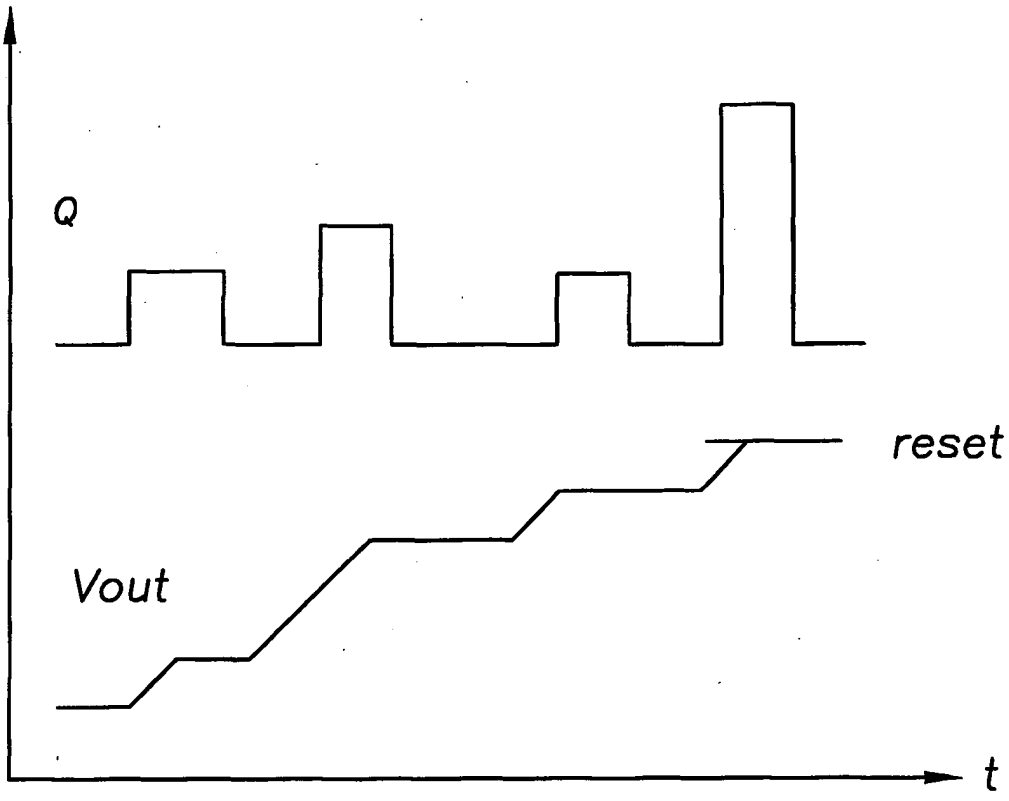
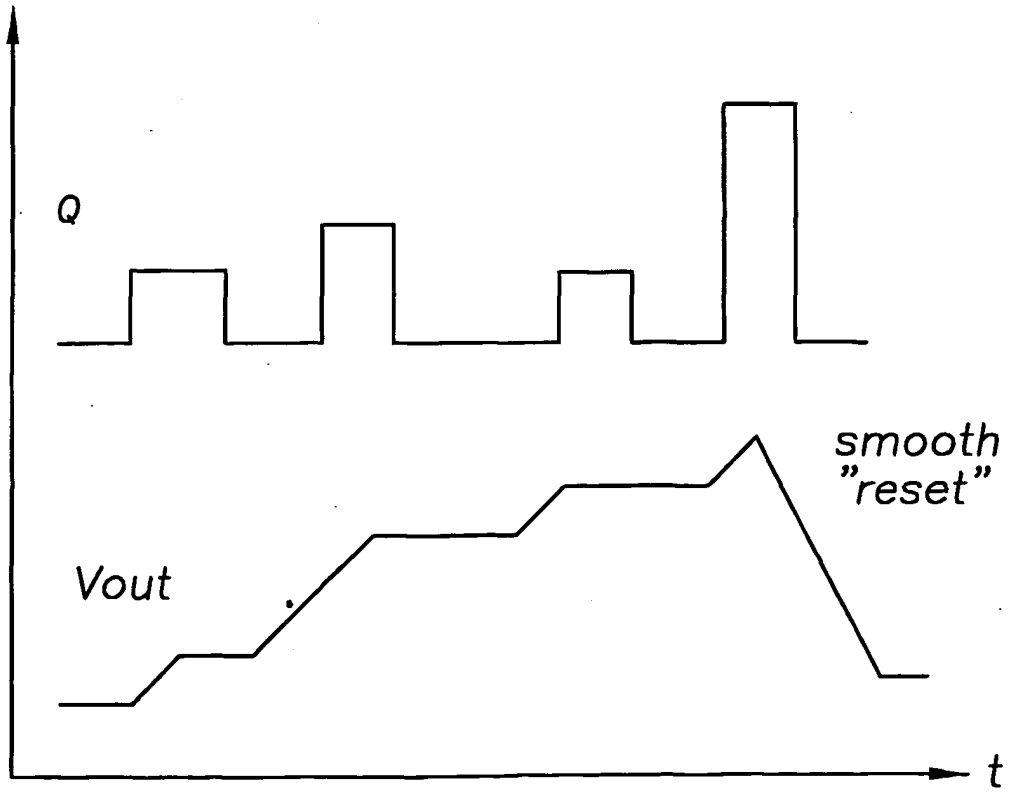


FIG. 16



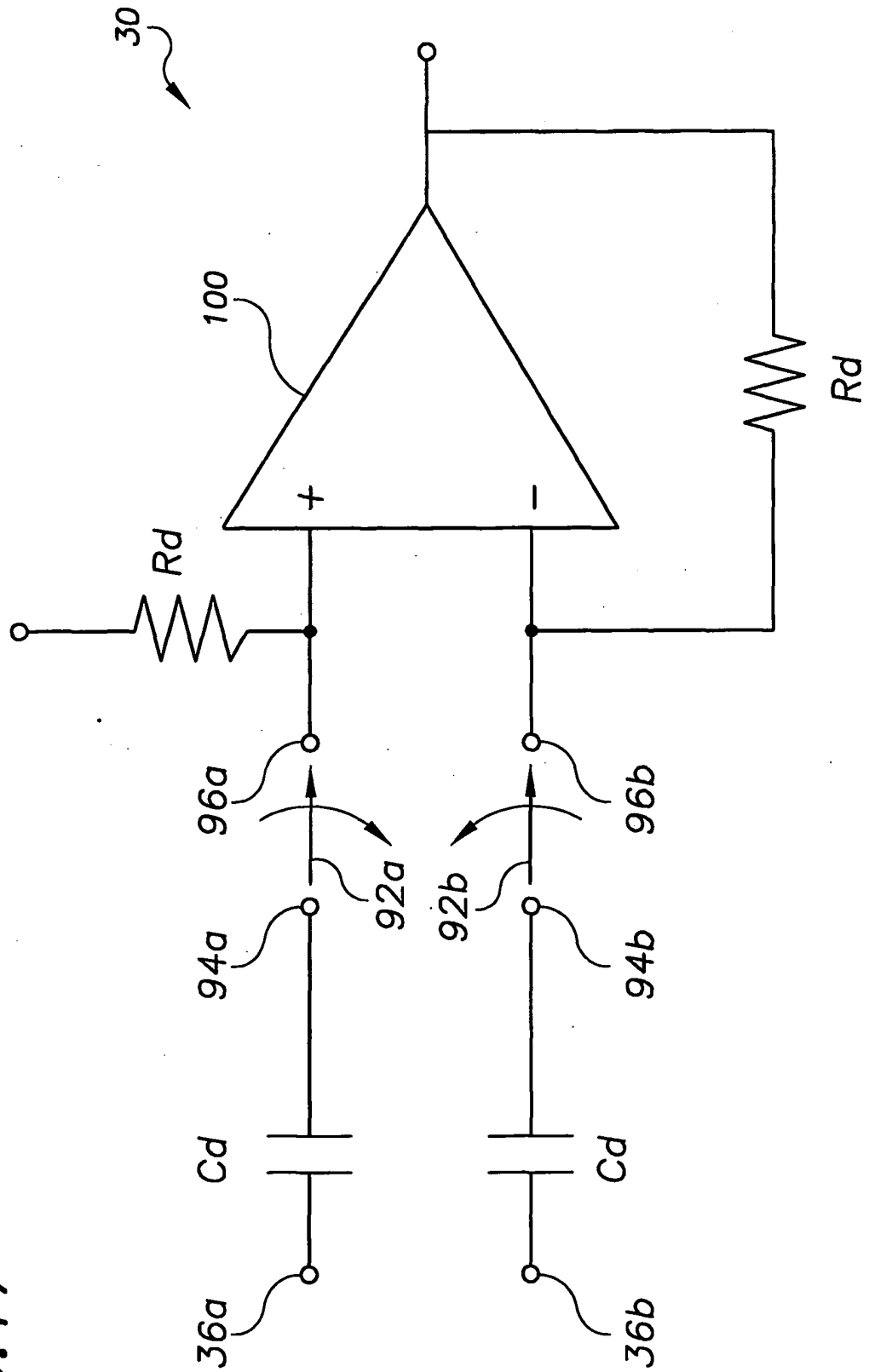


FIG. 17